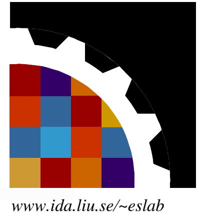
Linköping University
Embedded Systems Laboratory



Call for Participation in a SYDIC-Training Course on

Digital Systems Testing and Design for Testability

Course Contents

- Fault modeling and simulation.
- Automatic test pattern generation.
- Basic principles of design for testability.
- Testability analysis.
- Testability enhancement techniques.
- Test synthesis.
- Testability issues in hardware/software systems.
- Built-in self-test and special BIST architectures.

Course Organization

Part I: Lectures (16 hours)

1. Introduction and fault modeling and simulation

- General introduction
- Fault modeling
  - Logical level fault modeling; Fault equivalence and fault dominance; RT and high level fault models
- Fault simulation
- Test cost trade-offs

2. Automatic test pattern generation (ATPG)

- Basic theory of testing and test pattern generation
  - Boolean Derivatives; BDD and design modeling
- Test pattern generation methods
  - Gate-level test generation; D-Algorithm; Basic idea of PODEM; Functional test generation; Hierarchical test generation techniques
- Test generation of sequential circuits

3. Design for testability

- Basic principles
- Ad hoc solution, including test point insertion.
- Scan techniques, theory and practice
- Partial scan selection

Objective

To study the basic principles and practice of test technology and design-for-testability methods for digital systems. To address also issues related to the integration of test consideration with system synthesis and to system-on-chip testing.

Target Audience

Designers and test engineers interested in hardware testing and design for testability techniques for digital systems.

Duration

3 days.

Date

March 3-5, 2004.

Venue

Linköping University, Sweden.

Organizer

Prof. Zebo Peng.

Registration and contact

Email to zpe@ida.liu.se

4. Test synthesis and related issues

- Testability analysis techniques
- High-level test synthesis
- Board and system level test issues
- Core-based SoC test
  - Test scheduling; Test infrastructure design; Test power management
- Advanced issues

5. Built-in self-test

- Generic requirements for BIST
- Theory of pseudo-random generation as tests
- Response compression
- Special BIST Architectures
- Hybrid BIST and its optimization

6. Testability issues in hardware/software systems

- Heterogeneous systems and their design process
- Design validation and formal verification
- Design validation by model execution - design testing
  - Levels of testing; Functional vs. structural testing; Path testing; Transaction flow testing; Data-flow testing; Transition testing; Mutation testing; Testability metrics
- Hardware/software co-design for testability.

Part II: Lab Exercise (8 hours)

The lab exercise is intended to give some hands-on experience with commercial test and design for testability (DFT) tools. We will illustrate the features of such tools and show their placement with respect to the overall design flow. The exercises are performed with Mentor Graphics FastScan ATPG tool suite.

The first part of the exercise concentrates on test pattern generation and fault simulation. These concepts will be illustrated based on realistic design examples. The exercise will also illustrate how these tools fit into the overall design flow.

The second part of the exercise deals with design for testability. In particular, one of the mainstream DFT technologies—scan insertion—will be used in the exercise. We will study the practical aspects of scan insertion and learn how test generation can efficiently be performed for scanned circuits.

The course is given in the framework of the EU project IST-2001-35100 SYDIC-Training. Additional information can be found at

www.ecsi.org

Embedded Systems Laboratory
Dept. of Computer and Information Science
Linköping University

SE-581 83 Linköping
Sweden

Phone: +46 13 28 20 67
Fax: +46 13 14 22 31
E-mail: zpe@ida.liu.se

www.ida.liu.se/~eslab